REMARKS

Claims 1-32 are pending. Claim 8 was objected to. Claims 1, 4-8, 11-15, 18-19, 21, 23, 26-28, and 30 were rejected under 35 U.S.C. 102(e) as being anticipated by Squires (U.S. Patent No. 6,510,548). Claims 2-3, 9-10, 16-17, 20, 24-25, 29, and 32 were rejected under 35 U.S.C. 103(a) as being obvious over Squires in view of Ting (U.S. Patent No. 5,457,410). Claims 22 and 31 were rejected under 35 U.S.C. 103(a) as being obvious over Squires in view of Andrew (IEEE Explorer article "A field programmable system chip which combines FPGA and ASIC circuitry"). The Applicant's respectfully traverse the Examiner's objections and rejections.

Objections

Claim 8 has been amended to remove the duplicative phrase "that interfaces" which was due to a clerical error and hence the objection should be withdrawn.

Rejections under 35 U.S.C. 102(e)

Squires discloses providing a soft "core" that can be incorporated in an FPGA. This core is a predetermined set of configuration bits that will program a section of the FPGA to perform pre-designed functions (col. 1, lines 28-36, and lines 56-60). For example, a microprocessor function, can be either in a "hard" implementation such as an IBM PowerPC, or a "soft" implementation such as an FPGA programmed to perform the functions of a microprocessor (col. 1, lines 62-67). Squire does not disclose nor teach a method for incorporating a hard implementation in an FPGA.

Claim 1 recites among other features identifying an approximate number of configurable logic blocks and at least one fixed logic circuit. The fixed logic circuit is application

specific integrated circuit (ASIC) circuitry (support is found in p. 2, lines 5-16 of the specification) and is not part of the approximate number of configurable logic blocks. The fixed logic circuit of claim 1 is not a soft core as disclosed in Squire. Hence the Office Action's assertion that a fixed logic circuit includes the soft "core" of Squires is not correct. For at least this reason alone claim 1 should be allowable.

In independent claims 8, 15, and 23 the term fixed logic circuit is also not a soft core as described in Squires. For at least the same reasons as claim 1 is allowable, claims 8, 15, and 23 should be allowable.

Claims 2-7, 9-14, 16-22, and 24-32 being dependent upon claims 1, 8, 15, and 23, respectively, should be allowable for at least the same reasons claims 1, 8, 15, and 23 are allowable.

Rejections under 35 U.S.C. 103(a)

This application (10/092,051) and U.S. patent No. 6,510,548 (Squires) were at the time the invention of this application was made, commonly owned by Xilinx, Inc.. Hence, Squires is disqualified from being used in a rejection under 35 U.S.C. 103(a). At least for this reason alone claims 2-3, 9-10, 16-17, 20, 22, 24-25, 29, 31, and 32 should be allowable.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on October 17, 2003.

Pat Slaback
Name

Signature